Abstract

A processor includes scheduling circuitry for scheduling data blocks for transmission from multiple transmission elements, and traffic shaping circuitry coupled to the scheduling circuitry and operative to establish a traffic shaping requirement for the transmission of the data blocks from the transmission elements. The scheduling circuitry is configured for utilization of at least one time slot table which includes multiple locations, each corresponding to a transmission time slot. The scheduling circuitry is operative in conjunction with the time slot table to schedule the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement established by the traffic shaping circuitry even in the presence of collisions between requests from the transmission elements for each of one or more of the time slots. In an illustrative embodiment, the scheduling circuitry utilizes a transmission element linking mechanism in conjunction with a set of pointers to accommodate multiple transmission elements which request the same time slot.